REMARKS

In the outstanding Final Office Action, claim 32 was rejected under 35 U.S.C. §101, as being directed to non-statutory subject matter. Claims 25-35 were rejected under 35 U.S.C. §103(a) over SATO (U.S. Patent No. 5,956,328), in view of Applicant's disclosed prior art.

The Rejection of Claim 32 Under 35 U.S.C. §101

Applicant traverses the rejection of claim 32 under 35 U.S.C. §101. Upon entry of the present amendment, claim 32 will have been newly cancelled without prejudice to or disclaimer of the subject matter recited therein. Entry of the present amendment is believed proper at least because cancellation of claim 32 renders moot the rejection of claim 32 under 35 U.S.C. §101, and reduces the issues outstanding should this matter proceed to appeal. The herein-contained cancellation of claim 32 should not be considered an indication of Applicant's acquiescence as to the propriety of either outstanding rejection. Rather, Applicant has cancelled claim 32 in order to advance prosecution and obtain early allowance of claims in the present application.

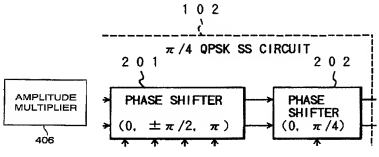
Applicant submits that the rejection of claim 32 under 35 U.S.C. §101 is rendered moot by the cancellation of claim 32. Therefore, withdrawal of the rejection of claim 32 under 35 U.S.C. §101 is respectfully requested.

The Rejection of Claims 25-35 Under 35 U.S.C. §103(a)

Applicant traverses the rejection of claims 25-35 under 35 U.S.C. §103(a). In this regard, the outstanding Final Office Action suggests that Applicant has misinterpreted the Examiner's proposed combination of SATO and Applicant's disclosed prior art. However, the Examiner has not provided any interpretation of how SATO and Applicant's disclosed prior art would be

combined such that Applicant's claims would result. Accordingly, Applicant's previously-provided interpretation of the proposed combination of SATO and Applicant's disclosed prior art is the only interpretation so far in the record, and there is no proper explanation in the record to justify the rejection over SATO in view of Applicant's disclosed prior art. Nevertheless, below Applicant will provide explanations on possible combinations of SATO and Applicant's disclosed prior art, and explain how each such combination does not result in the combination of Applicant's claims. **If this rejection is again maintained, the Examiner is requested to provide a detailed explanation that counters the explanation below, and explains her view as to how SATO in view of Applicant's disclosed prior art would result in Applicant's claimed invention.**

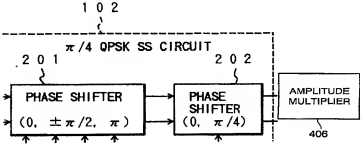
A modification of SATO with teachings of Applicant's disclosed prior art could result in a configuration as follows:



That is, the amplitude multiplier 406 in Applicant's disclosed prior art could be placed in front of QPSK spreading circuit 102 in SATO, and then signal amplifier 106 could be eliminated. Explained in the alternative, if SATO were used to modify Applicant's disclosed prior art, QPSK spreading circuit 102 in SATO would be used to replace the phase offset calculator 407 in Applicant's disclosed prior art. However, this configuration would not result in Applicant's claimed invention.

By way of explanation, phase shifters 201 and 202 of QPSK spreading circuit 102 in SATO (see Figures 1 and 2) are directed only to features of phase control, and not to amplitude adjustment. Therefore, QPSK spreading circuit 102 is entirely consistent with and analogous to phase offset calculator 407 in Applicant's disclosed prior art. A modification of QPSK spreading circuit 102 with Applicant's disclosed prior art would involve nothing more than a replacement of QPSK spreading circuit 102 with phase offset calculator 407, and a modification of phase offset calculator with SATO would involve nothing more than a replacement of phase offset calculator 407 with QPSK spreading circuit 102. These combinations of SATO and Applicant's disclosed prior art would not result in Applicant's claimed invention.

As an alternative to the modification of SATO set forth above, SATO could also be modified in the following manner:

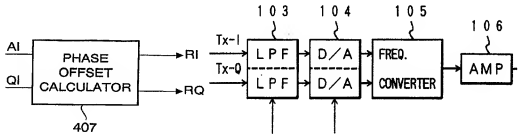


Explained in the alternative, phase offset calculator 407 in Applicant's disclosed prior art could be replaced with QPSK spreading circuit 102 from SATO, and QPSK spreading circuit 102 in SATO would then be placed in front of amplitude multiplier 406 in Applicant's disclosed prior art rather than behind amplitude multiplier 406. However, these combinations of SATO and Applicant's disclosed prior art would also not result in Applicant's claimed invention.

With respect to the configuration immediately above, Figure 1 of SATO already shows power amplifier 106 after the QPSK spreading circuit 102, so there is no reason to replace power

amplifier 106 in SATO with amplitude multiplier 406 in Applicant's disclosed prior art. Nevertheless, any such combination of SATO and Applicant's disclosed prior art also would not result in Applicant's claimed invention.

Another possible combination of SATO and Applicant's disclosed prior art would result in a configuration such as the following:



That is, phase offset calculator 407 in Applicant's disclosed prior art might replace QPSK spreading circuit 102 in SATO. However, this also would not result in the combination recited in Applicant's claims.

As set forth above, any simple modification of SATO with teachings of Applicant's disclosed prior art would simply replace an amplitude adjuster 106 in SATO with amplitude multiplier 406 in Applicant's disclosed prior art, or QPSK spreading circuit 102 of SATO with phase offset calculator 407 in Applicant's disclosed prior art. However, any such replacements/modifications would not result in the combination recited in Applicant's pending claims.

Therefore, no combination of SATO and Applicant's disclosed prior art would result in the combination of Applicant's claims. As set forth above, no such combination of SATO and Applicant's disclosed prior art results in Applicant's claimed invention, and the rejection of Applicant's claims on this ground should therefore be withdrawn.

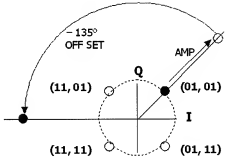
Applicant notes that benefits of the claimed invention were set forth in Applicant's previous Response. In this regard, Figure 7 of the present application generally illustrates features of offset processing in 45° units between -135° and 45°.

According to the invention to which Applicant's claims are directed, information (i.e. IQ data) is represented with two bits prior to amplitude multiplication processing. The two bits are sufficient to identify which of four quadrants QPSK IQ data lies in. However, amplitude multiplication is performed with respect to IQ data prior to 45° offset processing, and significant figures are increased. Afterwards, by performing a $\sqrt{2}$ calculation and rounding the fractions, the positions of IQ symbol points are represented with 45° offset applied. Offset processing in 90° units can be applied to two-bit information prior to amplitude multiplication.

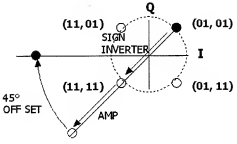
The following illustrations graphically explain differences in offset processing according to the embodiment of the claimed invention shown in Figure 4A and detailed in Figure 7, in comparison to the prior art shown in Figure 4B (note: the functional differences can be seen by following the directional arrows). As can be seen, simply switching on and off between offset processing in 90° units by changing the signs of symbol points in Sign Inverter 60 and offset processing in 45° units in 45° Phase Shifters requires only one $\sqrt{2}$ calculation, whereas the Prior Art offset processing requires multiple such $\sqrt{2}$ calculations.

Prior art	**(I, Q) →**	**1. Amplitude Multiplication →** **2. -135° Offset**
This invention	**(I, Q) →**	**1. 180° Offset (Sign Inverter) →** **2. Amplitude Multiplication →** **3. +45° Offset (on/off)**

PRIOR ART (FIG.4B)



THIS INVENTION (FIG.4A)



The following differences in data to be represented in processing are shown in the following table. The exemplary data for IQ symbol points are explained in tables as follows for the claimed invention in comparison to the prior art shown in Figure 4B:

▼FIG. 4A

INPUT (SCI, SCQ)	OFF SET VALUE	SIGN INVERTER (SRI, SRQ)	AMPLITUDE MULTIPLICATION (AI,	QI)	45°STEP PROCESSING (√2) on/off (RI,	RQ)
(01, 01)	+180	(11, 01) } (+180°)	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	-135	(11, 01) }	SRI * AMP	SRQ * AMP	AI * cos(45)	QI * cos(45)
(01, 01)	-90	(01, 11) } (-90°)	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	-45	(01, 11) }	SRI * AMP	SRQ * AMP	AI * cos(45)	QI * cos(45)
(01, 01)	0	(01, 01) } (0°)	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	+45	(01, 01) }	SRI * AMP	SRQ * AMP	AI * cos(45)	QI * cos(45)
(01, 01)	+90	(11, 11) } (+90°)	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	+135	(11, 11) }	SRI * AMP	SRQ * AMP	AI * cos(45)	QI * cos(45)

▼FIG. 4B

INPUT (SRI, SRQ)	OFFSET VALUE	AMPLITUDE MULTIPLICATION (AI,	QI)	45°STEP PROCESSING (RI,	RQ)
(01, 01)	+180	SRI * AMP	SRQ * AMP	AI * cos(180)	QI * sin(180)
(01, 01)	-135	SRI * AMP	SRQ * AMP	AI * cos(-135)	QI * sin(-135)
(01, 01)	-90	SRI * AMP	SRQ * AMP	AI * cos(-90)	QI * sin(-90)
(01, 01)	-45	SRI * AMP	SRQ * AMP	AI * cos(-45)	QI * sin(-45)
(01, 01)	0	SRI * AMP	SRQ * AMP	AI	QI
(01, 01)	+45	SRI * AMP	SRQ * AMP	AI * cos(45)	QI * sin(45)
(01, 01)	+90	SRI * AMP	SRQ * AMP	AI * cos(90)	QI * sin(90)
(01, 01)	+135	SRI * AMP	SRQ * AMP	AI * cos(135)	QI * sin(135)

As can be seen, the prior art requires multiple √2 calculations and associated processing, whereas the claimed invention according to Figure 4A and detailed in Figure 7 requires only a

single such $\sqrt{2}$ calculation. SATO as modified by Applicant's disclosed prior art would not result in Applicant's claimed invention, and would not result in the reduction in calculation processing achieved by Applicant's claimed invention.

If amplitude multiplication is performed before offset processing in 90° units, as in the Prior Art of Figure 4B, offset processing in 90° units will be performed with respect to a greater volume of information than two bits (e.g., 18 bits), and the amount of calculation will necessarily increase. Thus, by performing amplitude multiplication processing after offset processing is performed in 90° units, and before offset processing is performed in 45° units, as in the claimed invention shown in the embodiment of Figure 4A and detailed in Figure 7, it is possible to reduce the calculation amount in comparison to the prior art shown in Figure 4B. SATO as modified by Applicant's disclosed prior art does not result in Applicant's claimed invention (see the exhaustive explanation of possibilities set forth above), and does not result in the benefits of Applicant's claims as set forth above. A combination of Applicant's disclosed prior art and SATO does not result in Applicant's claimed invention and neither SATO nor Applicant's disclosed prior art provides any consideration of the amount of processing/calculation, and do not invite any modification in any manner such that the invention recited in Applicant's claims would be obtained. Such modification is not merely a matter of design choice, and the differences in inputs between the embodiment of Figure 4A and the prior art of Figure 4B have great significance which is arbitrarily dismissed in the rejection as state.

Therefore, according to the presently claimed invention, amplitude multiplication processing is performed after offset processing in 90° units, and before performing 45° offset processing, for the reasons described above, and the manner of this processing is not an obvious

variation that one of ordinary skill in the art would have been led to by SATO and/or Applicant's disclosed prior art.

At least for these reasons, SATO in view of Applicant's disclosed prior art do not render obvious independent claims 25, 26 and 28, each of which includes features relating to amplitude adjustment after sign inversion to obtain a first phase offset, and before phase offsetting by a second phase offset smaller than 90°. Benefits of the order in this processing relate to the amount of data required for representing and processing signals, and are not a subject rendered obvious or even taken into consideration by SATO and/or Applicant's disclosed prior art.

Therefore, the rejection of claims 25, 26, 28 and 32 under 35 U.S.C. §103 is improper, at least for each of the reasons set forth above.

Additionally, each of independent claim 28 and independent claim 33 recite features of controlling the second phase offsetting based on a signal from a remote source (in claim 28 "a message included in a reception signal from a receiver that receives communication signals" from the claimed CDMA transmission apparatus). There is no feature of SATO or Applicant's disclosed prior art that discloses controlling the second phase offsetting based on a signal from a remote source. Accordingly, SATO as modified by Applicant's disclosed prior art would not result in the combinations of claims 28 and 33, including controlling the second phase offsetting based on a signal from a remote source.

Accordingly, the rejection of claims 28 and 33 under 35 U.S.C. §103 is improper, at least for each of the additional reasons set forth above.

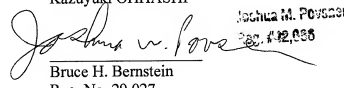
At least for the reasons set forth above, each of the independent claims now pending is allowable over SATO and/or Applicant's disclosed prior art, whether considered alone or in any proper combination. Further, each of the pending dependent claims is allowable at least for

depending, directly or indirectly, from an allowable independent claim, as well as for additional reasons related to their own recitations.

Accordingly, reconsideration and withdrawal of the outstanding rejections is requested.

Should there be any questions, any representative of the U.S. Patent and Trademark Office is invited to contact the undersigned at the telephone number provided below.

Respectfully submitted,
Kazuyuki OHHASHI



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